**Zhejiang University**

**Advanced Computer Architecture, Fall-Winter 2013**

**Final Exam**

Student ID\_\_\_\_\_\_\_\_\_\_\_\_Name\_\_\_\_\_\_\_\_\_\_\_\_ Grade\_\_\_\_\_\_\_\_\_\_\_\_

**Section One: You are required to choose the best answer from the four given choices marked A,B,C and D. Then mark your answer.(2 points \* 10)**

1.Michael Flynn [1966] looked at the parallelism in the instruction and data streams called for by the instructions at the most constrained component of the multiprocessor, and placed all computers into one of four categories.Array processors and vector processors is the [representative](javascript:void(0);)s of () while multi-processors system is the [representative](javascript:void(0);) of ().

A. SISD,SIMD B.SIMD,MIMD C.MISD,MIMD D.MIMD,SIMD

2.Forwarding can solve some data hazards,but not all potential data hazards can be handled by forwarding. Look at the sequence of instructions bellow, which stall can’t be eliminated by forwarding.( )

A. DADD R1,R2,R3 B. LD R1,0(R2)

DSUB R4,R1,R5 DSUB R4,R1,R5

C. DADD R1,R2,R3 D. LD R4,0(R1)

LD R4,0(R1) DADD R1,R2,R3

3. The relevance of the next followed instructions contains \_\_\_\_\_\_\_ 、\_\_\_\_\_\_\_\_ , and hazard which may occur in MIPS are \_\_\_\_\_\_\_、\_\_\_\_\_\_\_\_.

DADDIU R1,R3,# -8

BNE R1,R2,LOOP

SUB R4,R4,#8

A.RAW,WAR; B.Real Correlation , Reverse Correlation ;

RAW,WAR RAW , transmission

C.Real Hazard , Control Hazard; D.RAW,WAW;

RAW , transmission RAW,WAW

4. Choose the right answer including all the right options.

①Poor parallism among instructions

②Limited contents of score board

③Limited Function Units and Types

④Remained RAW && WAW Hazard

⑤Not considering forwarding

⑥Remained RAW Hazard

A.①②③④⑥ B.②③⑤⑥ C.①②③④⑤ D. ①③④⑤⑥

5. Tomasulo's scheduling algorithm mainly holds two advantages, the first one is\_\_\_\_\_\_\_ the logic of hazard checking , the second is eliminating the \_\_\_\_\_\_\_ hazard.

A. uniformed , WAW and WAR B. distributed , WAW and WAR

C. uniformed , WAW and RAW D. distributed , WAW and RAR

6.2-bit Branch-Prediction Buffer can reduce the cost of branch. Suppose the initial value of 2-bit Branch-Prediction Buffer is zero. There is a loop program with 10 times. If the former 9 branches of this loop program is taken and the last one is not taken. The hitting rate of predicting of the 2-bit Branch-Prediction is ( ). If the first branch is taken and the transfer behavior is changed every other branch, the hitting rate of predicting of the 2-bit Branch-Prediction is ( ).

A. 90% ,50% B. 70% ,20%

C. 70% ,50% D. 90% ,20%

7.The purpose of Multiple Issue Processor is that issue more than one instructions per clock. The two basic multiple-issue technologies is ( ) and ( ). Among them ( ) issue a fixed number of instructions formatted as one large instruction. ( ) mainly use hardware to detect hazard.

A. multiprocessor, superscalar; superscalar, multiprocessor

B. VLIW, superscalar; VLIW, superscalar

C. superscalar, VLIW; superscalar, VLIW

D. superscalar, VLIW; WLIW,superscalar

8.Choose the correct statement:

① In symmetric (shared-memory) multiprocessors (SMPs) architectures, all processors have different latency from memory, even if the memory is organized into multiple banks.

② In DSM architectures, a memory reference can be made by any processor to any memory location.

③ In Message-passing multiprocessors architectures, the same physical address on two different processors refers to two different locations in two different memories.

④ NUMAs’ (nonuniform memory access) memory access time depends on the location of a data word in memory.

A.①② B.①②③④ C.②③④ D.①③④

9.There are two different programs T1 and T2 sharing the same data.T1 use cache-1 and T2 use cache-2. Suppose cache use write-back way to write back data. The initial data of memory and cache and the program is listed in the table bellow. The data in the memory is ( ) when the program is executed.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Program T1 | Program T2 | Cache-1 | Cache-2 | initial data of memory | program |
| ST X,1  ST Y,10 | LD Y, R1  ST Y’,R1  LD X,R2  ST X’,R2 | X=  Y= | X=  X’=  Y=  Y’= | X=0  Y=5  X’=  Y’= | T1 is executed.  Cache-1 writes back X  T2 is executed  Cache-2 writes back X’and Y’  Cache-1 writes back Y |

A. X=1,Y=10,X’=1,Y’=5 B. X=0,Y=10,X’=1,Y’=5

C. X=1,Y=5,X’=1,Y’=10 D. X=0,Y=5,X’=1,Y’=5

10.In Directory-Based Cache Coherence Protocols, each cache block may be in one of the following three states: shared, uncached, exclusive. When the block is in the shared state, which requests can occur ? ( )

①Read miss②Write miss③Data write back

A.①②③ B.①② C.②③ D.①③

**Section Two: Give a short answer to the following questions.(4 points \* 5）**

1.Give a brief introduction of three types of pipeline hazards. Then point out the possible data hazards and approaches to solve the hazard.

2.Describe the theory of branch delay slot briefly and adjust the following codes according to it.

ADD R1,R2,R3

If R2 = 0 then

Delay slot

3.Describe the theory of Hardware-Based Speculation and function of ROB(Reorder Buffer) briefly.Then tell the functionality difference between ROB (Reorder Buffer) and reservation stations.

4.Tell the difference between Tomasulo algorithm and Scoreboard algorithm.

5.Have a brife introduction of Paralism

**Section Three: Calculating the following questions.(10 points \* 2）**

1) Have a brief introduction of Amdahl's Law

2) Assume the frequency of the FP( Float Point ) instructions is 25% , and its average CPI is 5.0, and the frequency of non-FP instructions is 2.33. FPSQR( Float Point square) instructions come up to 5%, and its average CPI is 20,

we have two kinds of Optimization Method to optimize this situation below,

1. Decrease the CPI of FPSQR to 2

2.Decrease the CPI of FP to 2.5

try to calculate the Average CPI of these two different methods respectively, the results are supposed to keep two significant digits.

3) Here we have 100 processor . In order to get the speed-up ratio at 50 , try to calculate the degree of parallelism of this community , the results are supposed to keep four significant digits.

2.The correlative parameters between commands are provided in the following table. Suppose We use a standard 5-level integer pipeline and these functional units are fully pipelined or copied. Try to analyze and calculate the following questions:

1. Without any scheduling, what the loop will execute? How many cycles it will take ?
2. Optimize the following codes using software pipelining compile method, to make it has the least hazards.
3. Compute How many cycles it will take after optimization.

|  |  |  |
| --- | --- | --- |
| Former operation | Successor operation | Clock Delay |
| FP ALU | FP ALU | 3 |
| FP ALU | Store (double word) | 2 |
| Load (double word) | FP ALU | 1 |
| Load (double word) | Store (double word) | 0 |

**Section Four:** **Analyzing the following questions.**

1.（15 points）Branch predictors that use the behavior of other branches to make a prediction are called correlating predictors or two-level predictors. In the general case, an (m,n) predictor uses the behavior of the last m branches to choose from 2m branch predictors, each of which is an n-bit predictor for a single branch. Now there is an (2,2) correlating predictor with 8K bits.

(1) How many entries are in this predictor?

(2) Draw the framwork of hardware of this predictor.

(3) Suppose the initial value of global transfer cache and every predictor is zero. The initial value of a is 1. What’s the hitting rate after run the program below 5 times by using this (2,2) correlating predictor?

Reg[R1]=a;

BNEZ R1,L1;

DADD R1,R0,#1;

L1: DADD R3,R1,#-1;

BNEZ R3,L2;

DADD R1,R0,#2

L2：…

if(a==0)

a=1;

if(a==1)

a=2;

2.（10 points）Assume the latencies for the floating-point functional units as follows: add is 2 clock cycles, multiply is 6 clock cycles, and divide is 12 clock cycles.

Using the code segment below, show what the status tables look like when the DIV.D is ready to go to commit.

L.D F6, 32(R2)

L.D F2, 44(R3)

MUL.D F0, F2, F4

SUB.D F8, F2, F6

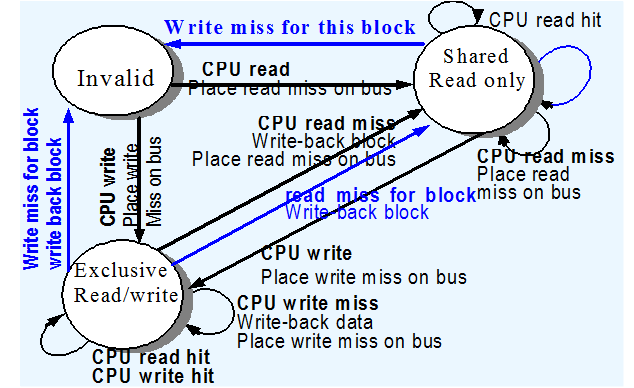
DIV.D F10, F0, F6

ADD.D F6, F8, F2

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Reorder buffer** | | | | |
| **Entry** | **Busy** | **Instruction** | **State** | **Destination** | **Value** |
| **1** |  |  |  |  |  |
| **2** |  |  |  |  |  |
| **3** |  |  |  |  |  |
| **4** |  |  |  |  |  |
| **5** |  |  |  |  |  |
| **6** |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **FP register status** | | | | | | | | | |
| **Field** | **F0** | **F1** | **F2** | **F3** | **F4** | **F5** | **F6** | **F7** | **F8** | **F10** |
| **ROB#** |  |  |  |  |  |  |  |  |  |  |
| **Busy** |  |  |  |  |  |  |  |  |  |  |

3.(15 points)Here is one SMP system , write invalidate and snooping-protocal based, supporting the cache coherence. Write cache data to memory by using “write-back” way. Fill the blanks below , relevant transmission relationships could be found according to the graph. (***NOTE:*** *while filling the* ***MEM*** *parts , if the answer is A1=10,A2=15 ,you should fill " A1 , A2 " in the Addr column and " 10 , 15 " in the Value column , and values are supposed to have the* ***same sequence*** *with Addr* )



***NOTE:*** *assume the initial state of Cache is Invalid ,and A1 and A2 are assumed to map to the same cache block.*

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | P1 | | | P2 | | | BUS | | | | MEM | |
| step | Stat | Addr | Value | Stat | Addr | Value | Stat | Proc | Addr | Value | Addr | value |
| **P2:Write 20 to A1** |  |  |  |  |  |  |  |  |  |  |  |  |
| **P1:Write 40 to A2** |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| **P2:Read A2** |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| **P1:Write 30 to A2** |  |  |  |  |  |  |  |  |  |  |  |  |
| **P1:Write 50 to A1** |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |